IN THE CLAIMS

1. (currently amended) A method for fabricating a silicon based package (SBP) in the sequence as follows:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

then forming an interconnection structure including multilayer conductor patterns over the first surface, then forming a protective overcoat layer over the interconnnection structure, and then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure, then thinning the reverse surface of the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP,

then forming via holes which extend through the UTSW, [and]

then forming metallization in the via holes with the metallization extending through the UTSW, and

then remove the temporary bond.

2. (previously presented) The method of claim 1 including bonding the metallization in the via holes to pads of a carrier.

3 . (previously presented) The method of claim 1 including forming capture pads on the first surface prior to thinning the wafer.

4. (previously presented) The method of claim 1 including:

initially forming capture pads on the first surface,

then forming the interconnection structure over the first surface and the capture pads,

then forming the temporary bond of the wafer holder to the reverse surface, and

then thinning the wafer, thereby forming the UTSW.

5. (previously presented) The method of claim 1 including:

initially forming capture pads on the first surface,

then forming interconnection structure over the first surface and the capture pads,

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW, and

then forming the via holes through the UTSW down to the capture pads.

6. (previously presented) The method of claim 1 including:

initially forming capture pads on the first surface,

then forming interconnection structure over the first surface and the capture pads,

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW,

then forming the via holes through the UTSW down to the capture pads,

then forming a dielectric layer over the surface of the wafer leaving the bottoms of the via holes clear with the capture pads exposed, and

then forming the metallization in the via holes in contact with the capture pads.

7. (previously presented) The method of claim 1 including:

initially forming capture pads on the first surface,

then forming interconnection structure over the first surface and the capture pads

then forming the temporary bond of the wafer holder to the reverse surface,

then thinning the wafer, thereby forming the UTSW,

then forming the via holes through the UTSW down to the capture pads,

then forming a dielectric layer over the surface of the wafer leaving the bottoms of the via holes clear with the capture pads exposed,

then depositing metal pads into the via holes in contact with the capture pads, and

then form metal joining structures on the metal pads.

8. (previously presented) The method of claim 1 including initially forming via holes in the first surface prior to thinning the wafer.

9. (previously presented) The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer covering the via holes.

10. (previously presented) The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes, and

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes.

11. (previously presented) The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes, and

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes.

12. (previously presented) The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes, and

then forming an interconnection structure over the first surface including the first metal layer.

13. (previously presented) The method of claim 1 including the steps as follows:

initially forming via holes in the first surface prior to thinning the wafer,

then forming a dielectric layer over the surface of the wafer including the via holes,

then forming a through via/cap pad layer of a first metal layer over dielectric layer including the via holes,

then planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming vias in the via holes, and

then forming interconnection structure over the first surface including the metal vias and the first metal layer,

then forming the temporary bond to the rigid wafer holder on the reverse surface, and

then thinning the wafer to the desired thickness of the UTSW.

14. (currently amended) A method for fabricating a silicon based package (SBP) comprising:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

then forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

then forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

then forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

then forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

then forming a protective overcoat layer over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

then thinning the reverse surface of the wafer to a desired thickness to form an ultra thin silicon wafer (UTSW) for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, and

then removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW, and

then removing the temporary bond.

15. (previously presented) The method of claim 14 including the steps of forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes, followed by planarizing the via/cap pad layer down to the surface of the dielectric layer, thereby forming the metal vias in the via holes.

16. (previously presented) The method of claim 14 including the steps of forming the metal vias by forming a blanket through via/cap pad layer of a first metal layer over dielectric layer including the via holes, followed by planarizing to remove the via/cap pad layer above the surface of the dielectric layer, thereby forming the metal vias in the via holes,

then forming the interconnection structure over the first surface including the metal vias and the first metal layer,

then forming the temporary bond to a rigid wafer holder on the reverse surface, and

then thinning the wafer to the desired thickness of the UTSW.

Claims 17-24 (canceled)

25. (previously presented) A method for fabricating a Silicon Based Package (SBP) in the sequence as follows:

starting with a wafer composed of silicon and having a first surface and a reverse surface which are planar as the base for the SBP,

then forming an interconnection structure including multilayer conductor patterns over the first surface,

then forming a protective overcoat layer composed of polyimide over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure,

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP,

then forming via holes which extend through the UTSW, [[and]]

then forming metallization in the via holes with the metallization extending through the UTSW, and

then removing the temporary bond.

26. (previously presented) The method of claim 25 including:

forming the temporary bond with polyimide, and

releasing the temporary bond by laser ablation.

27. (currently amended) [[A]] The method for fabricating ~~a silicon based package (SBP)~~ and SBP in accordance with claim 30 comprising:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are planar,

then forming via holes which extend partially through the wafer from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

then forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

then forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

then forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

then forming a protective overcoat layer composed of polyimide over the interconnnection structure,

then forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed,

then thinning the reverse surface of the wafer to a desired thickness to form ~~an Ultra Thin Silicon Wafer (UTSW)~~ the UTSW for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias, [[and]]

then removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW; and

then releasing the temporary bond.

28. (previously presented) The method of claim 27 including:

forming the temporary bond with polyimide, and

releasing the temporary bond by laser ablation.

Please add the following claims

29. (new) A method for fabricating a Silicon Based Package (SBP) from a silicon wafer which has a first surface and a reverse surface which are planar by thinning the reverse surface of the silicon wafer to form an Ultra Thin Silicon Wafer (UTSW) with a desired thickness by the following steps:

first starting with the silicon wafer as the base for the SBP,

then performing alternative sequences of the steps which follow:

forming a temporary bond between the silicon wafer and a wafer holder leaving the reverse surface exposed, with the wafer holder being a rigid structure,

forming via holes deep enough to extend from the first surface to the desired thickness in the silicon wafer prior to the step of thinning the reverse surface of the wafer, and subsequently filling the via holes with metallization, and

thinning the reverse surface of the wafer to a desired thickness to form the UTSW for the SBP, and

thereafter releasing the temporary bond.

30. (new) The method of claim 29 including the steps performed in the sequence as follows:

performing a step of forming an interconnection structure including multilayer conductor patterns over the first surface of the silicon wafer;

then forming a protective overcoat layer over the interconnnection structure,

then forming the temporary bond between the protective overcoat layer of the SBP and the wafer holder leaving the reverse surface exposed;

then thinning the reverse surface of the wafer to a desired thickness to form the UTSW for the SBP;

then forming via holes which extend through the thickness of the UTSW;

then forming metallization in the via holes with the metallization extending through the thickness of the UTSW; and

thereafter releasing the temporary bond.

31. (new) The method of claim 29 including the steps performed in the sequence as follows:

performing a step of forming via holes which extend partially through the wafer through the desired thickness of the UTSW from the first surface towards the reverse surface with the each via hole having a base thereof which is closest to the reverse surface,

then forming a dielectric layer covering the first surface of the silicon wafer and the via holes with distal portions of the dielectric layer being located at the bases of the via holes, so that the distal portions are closest to the reverse surface,

then forming metal vias in the via holes on the dielectric layer with proximal ends being located at the first surface and distal ends of the metal vias being located on the distal portions of the dielectric layer, thereby being closest to the reverse surface,

then forming an interconnection structure including multilayer conductor patterns over the metal vias and the dielectric layer,

then forming a protective overcoat layer over the interconnnection structure,

then forming the temporary bond between the protective overcoat layer of the SBP and a wafer holder, leaving the reverse surface of the wafer exposed,

then thinning the reverse surface of the wafer to a desired thickness to form the UTSW for the SBP exposing the distal portions of the dielectric layer covering the distal ends of the metal vias,

then removing the distal portions of the dielectric layer exposing the distal ends of the metal vias which extend through the UTSW, and

thereafter releasing the temporary bond.